IMPROVEMENTS ON A MOSFET MODEL FOR NON-LINEAR RF SIMULATIONS

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Abstract:

As the gate lengths of silicon MOSFETs become smaller and smaller, these devices are usable to frequencies in the GHz range. The non-linear MOSFET model presented in this paper is based on S-parameter measurements over a large bias range and has been implemented in a SPICE simulator. The improvements consist of new equations for the non-linear capacitances and output conductance of the MOS transistor. This new large signal model shows very good agreement between measurement and simulation up to 10 GHz.

Introduction:

Silicon device technology has become an attractive low cost solution for many high frequency personal communication products[1]. These analog applications require good high frequency models in order to predict the RF circuit performance with accuracy. The most widely used models of the MOS transistor are not particularly suited for high frequencies[2]. The model modification presented in this paper proposes new equations for the non-linear capacitances and the loss resistances of a MOS transistor. To simplify the implementation, the DC drain current equation of a SPICE LEVEL 3 model was used while the accuracy for RF simulations was achieved by adding the new capacitance equations using subcircuits. The combination of the DC and RF parts of the model predicts the non-linear high frequency performance up to 10 GHz over various bias points.

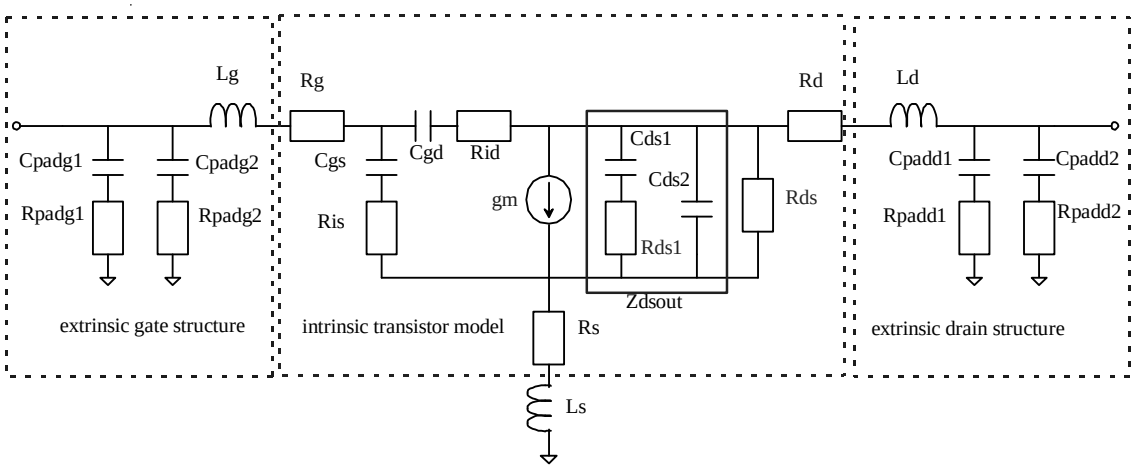

Figure 1: Small signal equivalent circuit used for the extraction of the linear intrinsic elements

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Modeling process:

In order to verify the proposed model improvements, test transistors on a 1 µm self-aligned contact CMOS (SACMOS) process from Philips Semiconductor with a total gate width of 300 µm with 20 fingers were used [3]. Small signal on wafer S-parameters have been measured for a transistor test structure at various bias points. These bias points ranged from 1V to 3V for the gate-source voltage and 0.2V to 4.5V for the drain-source voltage. The de-embedding of the extrinsic structures is described in [4]. The small signal intrinsic elements were extracted from this de-embedded data using a similar procedure as in [5]. The small signal equivalent circuit used is shown in Figure 1 [3].

The output conductance is modeled in two parts [6]: $1/R_{ds}$ and the Z_{dsout}. The $1/R_{ds}$ models the low frequency output conductance while the high frequency output impedance is dominated by C_{ds1}, C_{ds2} and R_{ds1} which combine to form Z_{dsout} (Fig. 1). Once the equivalent circuit element values of the linear model are known over all bias points, the next challenge is to find equations that fit the extracted capacitances over all bias points. This modeling process is shown in Figure 2.

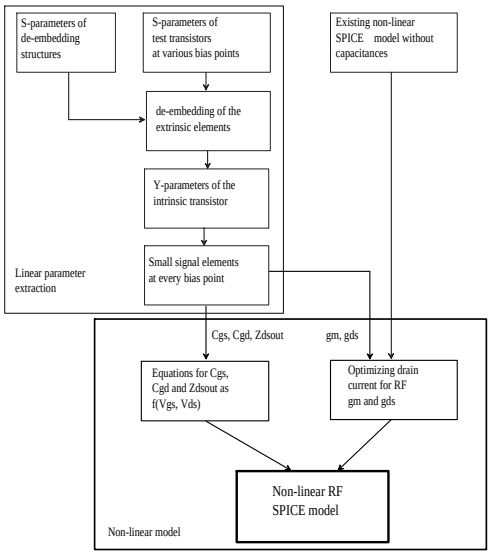

Figure 2: Flow chart of the modeling process used to obtain a non-linear RF SPICE model.

Improvement for the non-linear MOS model:

The model modification consists of new equations for the non-linear capacitances and the loss resistances of a MOS transistor. The equations presented are dependent on both the gate-source and the drain-source voltages. A hyperbolic tangent function was chosen to satisfy the shape of the capacitance and resistance curves as a function of the bias voltages. The C_{gs} capacitance equation is shown in Equation 1 and Fig. 3. The equations for the other capacitances are very similar to Equation 1.

$$C_{gs} = C_{gs0}\left\{1 + (0.284 - \frac{0.234}{V_{gs}^2})\tanh\left[V_{ds}\cdot(\frac{2}{V_{gs}-0.5} - \frac{4}{3} + V_{ds})\right]\right\} \quad (1)$$

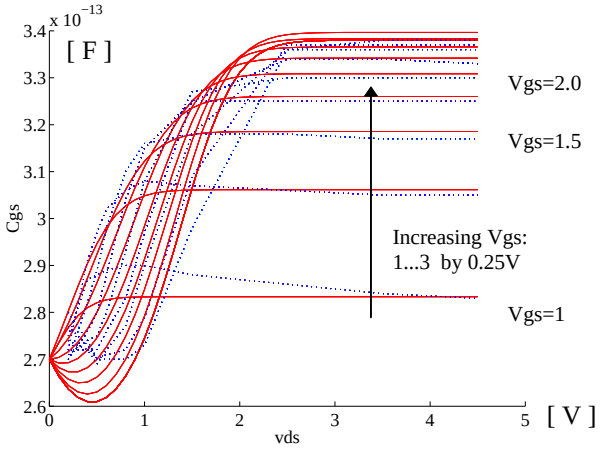

Figure 3: C_{gs} as a function of V_{ds} and V_{gs} dotted: extracted from measurements, solid: Equation 1.

Once the equations for C_{gs}, C_{gd}, and Z_{dsout} are determined, the implementation in a SPICE type simulator, in our case PSpice, is the next step. The interesting region of operation for high frequencies is the saturation region. Thus, this region has first priority when considering the accuracy of the model. For high frequency models, the most sensitive parameters are the capacitances and g_m [3]. To simplify the implementation, the DC current equation of a MOS LEVEL 3 was used and its g_m and g_{ds} optimized to match the measured

DC data especially in the saturation region. Simultaneously, the DC drain current in this region must also be considered.

The proposed equations for the non-linear capacitances were implemented using a subcircuit with a voltage controlled current source [7]. The new SPICE model consists of three external capacitances: C_{gs}, C_{gd} and Z_{dsout}, the series resistances and the non-linear current source of a LEVEL 3 transistor to model the g_m, g_{ds} and the DC current characteristics.

Results:

The simulations of this high frequency MOSFET model have shown very good agreement with the measurements over a wide range of bias points. The model is valid up to 10 GHz (Fig. 4) as can be seen by comparing the simulation and the measurements of all S-parameters at a typical bias point.

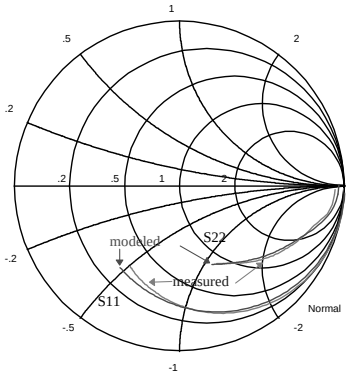

Figure 4 (a): Input and output reflection of modeled and measured transistor at $V_{gs} = V_{ds} = 1.5$, $I_d = 9.07$ mA, error=0.1047; Frequency range is from 50 MHz to 10 GHz.

An error function similar to the least squares error was defined in Equation 2. Various bias points were simulated and the error calculated.

$$\varepsilon_{tot} = \sum_{ij}\left\{\sum_{freq}\frac{\left|measS_{ij} - simS_{ij}\right|^2}{\left|measS_{ij}\right|^2}\right\}\frac{1}{N_{freq}} \quad (2)$$

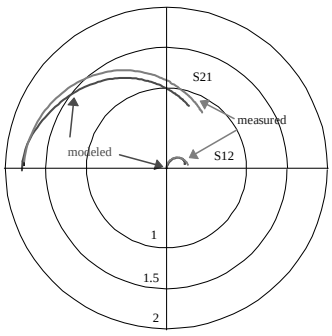

Figure 4 (b): Forward and reverse transmission of modeled and measured transistor at $V_{gs} = V_{ds} = 1.5$, $I_d = 9.07$ mA, error=0.1047; Frequency range from 50 MHz to 10 GHz.

The resulting error is small and fairly constant as long as the transistor is in the saturated region of operation (Fig. 5). More emphasis was placed on this region of operation while optimizing the DC drain current parameters. The error in the linear region is larger mostly due to the poorly modeled DC output conductance of the SPICE LEVEL 3 current model in these bias points.

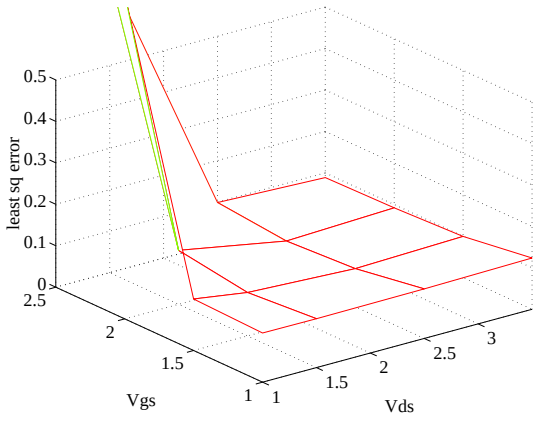

Figure 5: Error function defined in Equation 2 of the measurements versus PSPICE simulations over 16 different bias points.

To test the nonlinear performance of the model, the two tone intermodulation (IM) products of a transistor were measured and simulated. The input frequencies were chosen to be in the frequency range of interest for CMOS telecommunication applications (1.8 GHz).

The fundamental and third order IM both simulated (solid) and measured (dotted) are shown in Figure 6. The third order intercept point (IP3) for both cases is approximately 17.5 dBm. The accuracy of the third order intermodulation at low input power levels is degraded by the numerical accuracy of the simulations when using subcircuits. An implementation in C, directly in the SPICE code could increase the accuracy and reduce convergence problems caused by subcircuits.

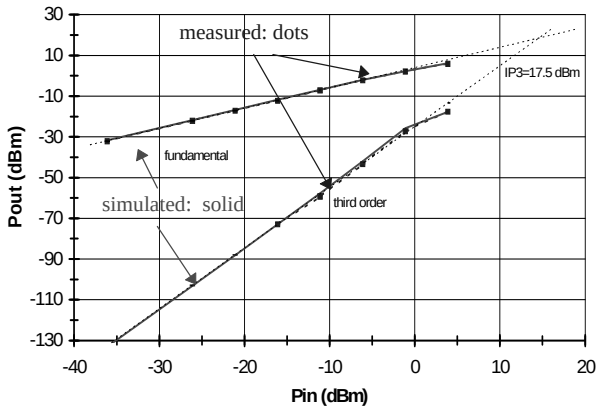

Figure 6: Two tone intermodulation of a single transistor of 300 μm gate width and 1 μm gate length Frequencies: 1.8 , 1.805 GHz, Bias point: Vgs=1.5, Vds=2.5, Id=9.3mA

Conclusions:

A non-linear high frequency MOSFET model has been developed for frequencies up to 10 GHz. The microwave frequency performance of the model has been investigated. The model is based on S-parameter measurements at various bias points. The simulations and measurements show good agreement over a wide range of bias voltages. As was shown with the third order IM simulations, the nonlinear behavior is also well modeled. The simple modification consisting of additional subcircuits is available in all SPICE simulators. As presented in this paper, these modifications significantly improve the high frequency performance of this model. This new model allows designers to simulate non-linear CMOS circuits up to 10 GHz with the accuracy previously limited to small signal simulations.

References:

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